Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	62	(transfer$3 near4 (data signal)) and ((clock near2 domain)) and (CPLD FPGA) and ("application specific integrated circuit")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/18 11:12
S1	7	((korger moss).in.) and (((ready begin start initiat$3 commence) near4 (indicat$3 display signal)) same clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/11 11:28
S2	3	((korger moss).in.) and (((ready begin start initiat$3 commence) near4 (indicat$3 display signal)) near9 clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/11 11:40
S3	19	((ready begin start initiat$3 commence) near4 (indicat$3 display signal)) near9 (clock same (("same" common) near4 frequency))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/11 11:55
S4	7	("60000037" "6033441" "6247082").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/11 11:56
S5	6	("6000037" "6033441" "6247082").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/11 13:12
S6	172	(clock near2 domain) same (data near4 (ready start indicat$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/11 13:14
S7	142	((clock near2 domain) same (data near4 (ready start indicat$4))) and synchroniz$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/13 07:27
S8	799	((serial cascad$3) near4 (processing (flip near2 flop))) same (transfer$3 near4 (data signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/13 12:01
S9	1841	((serial cascad$3) near4 (process$3 (flip near2 flop))) same (transfer$3 near4 (data signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/14 09:31
S10	142	((clock near2 domain) same (data near4 (ready start indicat$4))) and synchroniz$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/13 12:08
S11	2	S9 and S10	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/13 12:08

S12	2	((serial cascad$3) near4 (process$3 (flip near2 flop))) same (transfer$3 near4 (data signal)) and ((clock near2 domain) same (data near4 (ready start indicat$4)))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/14 09:32
S13	9	((serial cascad$3) near4 (process$3 (flip near2 flop))) same (transfer$3 near4 (data signal)) and ((clock near2 domain))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/14 10:12
S14	0	((serial cascad$3) near4 (process$3 (flip near2 flop))) same (transfer$3 near4 (data signal)) and ((clock near2 domain)) and (CPLD FPGA)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/14 10:13
S15	156	(transfer$3 near4 (data signal)) and ((clock near2 domain)) and (CPLD FPGA)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/14 10:13
S17	14	(transfer$3 near4 (data signal)) and ((clock near2 domain)) and (CPLD and FPGA) and ("application specific integrated circuit")	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/14 13:50
S18	18	(transfer$3 near4 (data signal)) and ((clock near2 domain)) and (CPLD and FPGA and ("application specific integrated circuit" ASIC))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/01/14 13:51